Design method of meta operators based on Equivalence class distribution

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Introduction

Currently, there are many physical systems for quantum computing. To adapt to the physical characteristics of different systems, engineers have designed different basic gate groups for gate circuit calculation models. The quantum algorithm realizes the evolution of the quantum state by applying unitary operators to the quantum states, and the results are obtained by measuring the outputs. The operators can only be done in the corresponding physical system by compiling and decomposing into hardware supported basic gates. Universal fundamental gates can construct all quantum algorithms, but their computational efficiency is limited. Drawing on the idea of meta operators in classical machine learning, by constructing a deep learning framework for deep learning models, the common computational logic of operators in different deep learning frameworks is abstracted as 'meta operators'. Used to discover errors in the training process of the model. Inspired by this idea, this article aims to study the common computational logic of quantum computing and proposes meta operators for quantum computing with geometric methods. Identify the optimal meta operator to optimize the depth of the circuits.

Method

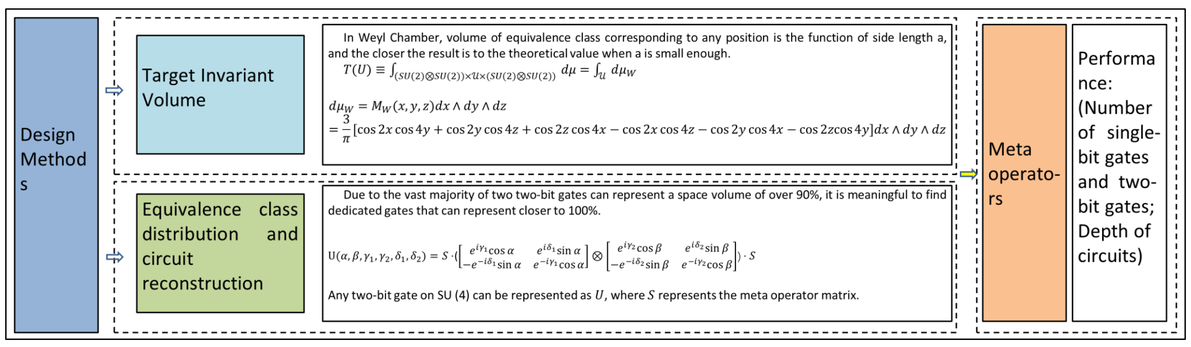

***FIGURE 1**. The design method of meta operators. It is divided into target invariant volume and Equivalence class distribution. The volume on Weyl Chamber needs to be calculated. After obtaining the best performing meta operator, verify its performance advantages on the algorithm circuit through experiments.*

In actual quantum gate measurement and control, it is impossible to accurately implement any gate in a true sense, and only approach this gate as close as possible in control. The quantum unitary operators within SU(4) requires 15 parameters $(x_1, \dots, x_{15})$ to be determined. Assuming that the exact values of the given gate are $(x'_1, \dots, x'_{15})$, the actual gate implemented by manipulation can only fall within the neighborhood of the exact values $(x'_1 \pm \delta_1, \dots, x'_{15} \pm \delta_{15})$. The smaller the value of δ_i, the closer it is to the exact value. The volume of this field provides a choice space for approaching this gate, and the larger the volume, the more targets available for selection. Increasing the range of parameters can the volume be expanded to facilitate the implementation of this gate, and the volume is called as target invariant volume. The calculation of invariant volume is obtained through integration, and this region is usually selected as the region within the Weyl Chamber of a small cube, whose length is parallel to the coordinate axis centered on (c_1, c_2, c_3). Since SU(4) is a non-smooth space with non-Euclid metric, it can be obtained by HAAR metric integration.

Since SU(4) is a non-smooth space with non-Euclid metric, it can be obtained by HAAR metric integration.$T(U) \equiv \int_{(SU(2)\otimes SU(2))\times U\times(SU(2)\otimes SU(2))} d\mu = \int_U d\mu_W, d\mu_W$ is the HAAR metric on $SU(4)$. In Weyl Chamber, volume of equivalence class corresponding to any position is the function of side length a, and the closer the result is to the theoretical value when a is small enough. The polynomial of function is the sum of some higher-order infinitesimals of a, while the smallest order represents the maximum upper bound. The larger the volume value, the larger the controlled area, and the easier it is to achieve precise control; On the contrary, the smaller the area, the more difficult it is to achieve precise control. The basic gate group of quantum computing is composed of single-bit and two-bit gates. The size of the space that can be represented by the combination of two dedicated gates and some single-bit gates is recorded as an indicator for evaluating the performance of this gate. The closer the spatial volume to 1, the stronger the representation ability of this gate. The better the performance of circuits composed of dedicated gates and some single bit gates.

Due to the vast majority of two two-bit gates can represent a space volume of over 90%, it is meaningful to find dedicated gates that can represent closer to 100%. Any two-bit gate on SU (4) can be represented as U, where S represents the meta operator matrix.

$$U(\alpha,\beta,\gamma_1,\gamma_2,\delta_1,\delta_2) = S\cdot(\begin{bmatrix} e^{i\gamma_1}\cos\alpha & e^{i\delta_1}\sin\alpha \\ -e^{-i\delta_1}\sin\alpha & e^{-i\gamma_1}\cos\alpha\end{bmatrix}\otimes\begin{bmatrix} e^{i\gamma_2}\cos\beta & e^{i\delta_2}\sin\beta \\ -e^{-i\delta_2}\sin\beta & e^{-i\gamma_2}\cos\beta\end{bmatrix})\cdot S$$

To compute the Characteristic polynomial of U, the method of undetermined coefficients can be used to determine the value range of (c_1, c_2, c_3). The intersection with Weyl Chamber is marked as W', which is the distribution domain of the equivalence class. The points in this field represent the range of that can be covered by two dedicated gates and some single-bit gates. The volume of the domain represents the compilation performance of U.

Results

According to geometric methods, the dedicated gate CPX2 and gate family CPX with the best performing are found. The meta operator is applied to reconstruct the circuit, which proves that the meta operator can optimize the circuits and analyzes the interaction between the circuit topology and the dedicated gates.

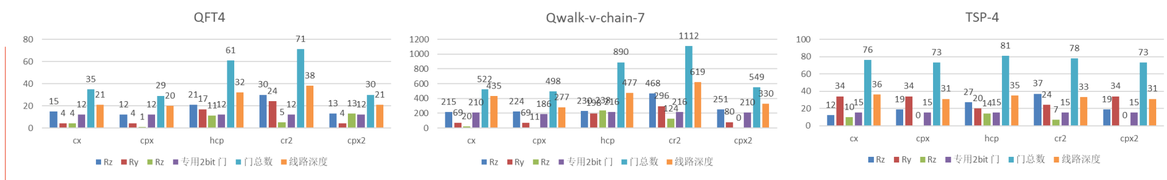

***FIGURE 2**. These figures are the performance under different algorithms using different dedicated gates and single-bit gates.*

Firstly, to compare the performance of the reconstructed circuit using gate CX and Cpx2. The number of two-bit gates used in these three circuits are same, but with the same overall depth of the circuits, CX requires more single-bit gates than Cpx2 in the QFT; In the Qwalk problem, Cpx2 uses 25% more single-bit gates than CX gates, but the depth of the circuit is about 24% shallower than CX gates. By using virtual Z-gate technology, the impact of increasing the number of single bit gates is smaller than the impact of increasing depth. In the TSP problem, the number and depth of single-bit gates used in the CX gate circuit are greater than those brought about using Cpx2 gates. From this, the depth optimization effect of Cpx2 gate on these types of problems is significant.

In addition, Cpx gates are a class of gates with parameters, where Cpx2 is a special case of Cpx gates. It is not difficult to see that in the circuits with the above problems, the performance of the Cpx gate family is better than that of Cpx2. Especially in the Qwalk problem, the number of two-bit gates or single bit gates used, as well as the depth are all optimal. This shows that this family performs very well in the optimization of these quantum circuits.

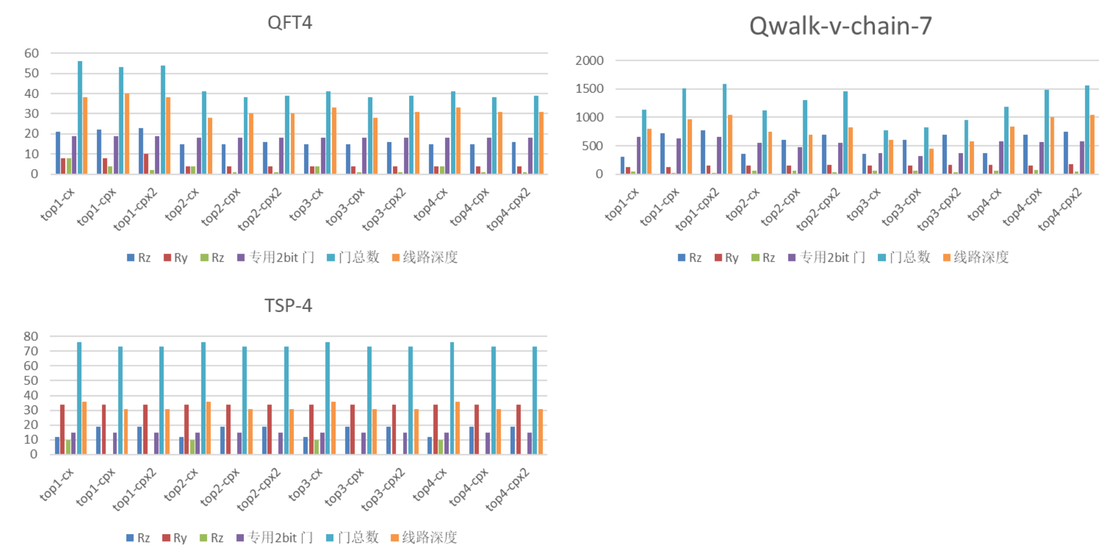

***FIGURE 4**. This is the performance analysis of meta operators in algorithm circuits QFT, Qwalk and TSP under four different topologies.*

In QFT circuit, topology 1, also known as linear topology, has a significant impact on QFT, leading to an increase in circuit depth and the total number of gates. Currently, the performance of dedicated gate Cpx2 is still the best. The remaining three topologies have little impact on the circuit of the dedicated gate, without causing an increase in the depth of the circuit and the total number of gates. Moreover, the performance of the dedicated gate Cpx2 is only affected in topology 2, which is a ring topology, while the performance of the other two topologies remains better than that of the CX circuit. In Qwalk circuit, it is known that topology 1, topology 2, and topology 4 have a significant impact on the Qwalk circuit, and the performance of the CX reconstructed circuit is the best under these topologies, while the performance of the dedicated gate Cpx2 is poor. The impact on the circuits is minimal under topology 3, and the performance of dedicated gate Cpx2 is better than that of the constructed circuit with CX.

TSP circuit shows that the impact of different topologies on the performance of TSP circuit is consistent with that under fully connected topology, and the performance of the dedicated gate Cpx2 reconstruction circuit is the best.

The above conclusion indicates that topology also has an impact on the performance of dedicated gate for circuits reconstruction. The performance of dedicated gates is related to topology, and the question of which dedicated gate to use in what topology is worth further research. On the contrary, dedicated gates also affect the topology of the algorithms, further providing guidance for the topology design of the chip.

Conclusions & Perspectives

- ❖ The performance of meta operators was evaluated in TSP, Qwalk, and QFT circuits, and compared with other operators, it was proven that the found operator is optimal.
- ❖ In both fully connected and non fully connected topologies, it can be seen that different topologies have different impacts on the performance of dedicated gate Cpx2 in several problems. However, this type of gate family CPX still maintains optimal performance.
- ➢ ToDo: High dimensional quantum element operators can be worth further research
- ➢ Design and implement dedicated quantum gates based on the matrix of meta operators

Acknowledgements

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